Skyrmion based logic-in-memory devices

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Fast, high-density, and energy-efficient devices are crucial enablers of today's IT technology pushed by the advent of cloud computing, big data, and the internet of things. To face this challenge, the conventional Von Neumann architecture where logic and memory units are separately implemented leads to critical issues: the increase of the length of the global interconnects between the logic and memory units when downscaling results in a critical rise in power and delay. A promising alternative lies in "Logic-In-Memory" (LIM) architectures that merge logic and memory functions in the same device promising non-volatility, ultra-low-power, and high-speed operations. Topological magnetic textures called skyrmions are ideally suited for this purpose due to their nanoscale size, fast motion, and non-volatility. They also repel each other which can be leveraged to perform basic logic operations. Several proposals have been presented in the past for skyrmion-based logic gates [1][2], however, most of these require an intermediate conversion of magnetic information to electrical signals which is inefficient for large-scale computation where several levels of cascading is often required to perform complex operations. In this study, by using micromagnetic simulations, we present a Synthetic Antiferromagnet based LIM architecture that relies purely on magnetic interactions for performing logic operations. We first design a racetrack storage that uses skyrmions as memory bits confined by anisotropy energy barriers and outline simple protocols for "nucleate" and "Shift" operations on skyrmions using current-induced spin-orbit torques. We then combine our racetrack storage with a newly designed 1-bit Full Adder (FA) gate extendable to n-bit FA by cascading. The designed FA is reprogrammable and can also be used to perform AND/OR/NOT/NAND/XOR/XNOR operations. We discuss the performance metrics of the FA gate along with its electrical tolerances and show that the device performs well even with some fluctuations in the amplitude/width of the injected current pulse. The monolithic design of the logic gate and the absence of any complex electrical contacts makes the device ideal for integration with conventional CMOS circuitry.

[1] S. Luo and L. You, APL Materials, Vol. 9, p.050901 (2021)
[2] S. Li, W. Kang, X. Zhang et al., Mater. Horiz., Vol. 8, p.854-868 (2021)